IN THE SPECIFICATION:

Please amend the specification as follows.

Amend the paragraph spanning from p. 1, ln. 29, to p. 2, ln. 17 as follows:

Many techniques for efficiently implementing the emulation circuit have been developed. For example, U.S. Patent 5,761,484, entitled "Virtual Interconnections for Reconfigurable Logic Systems" to Agarwal et al., provides an efficient method to route signals between the PLDs by "multiplexed data transport," i.e., sharing input or output pins among many input or output signals. In one implementation of that system, a clock signal ("virtual clock") of many times the frequency of the system clock is used for these input and output signals. U.S. Patent 5,854,752, entitled "Circuit Partitioning Technique For Use With Multiplexed ~~Intereconnections~~Interconnections" to Agarwal, provides an efficient way of circuit partitioning that achieves high utilization of the available resources in the PLDs. U.S. Patents 5,659,716 and 5,850,537, both entitled "Pipelined Static Router And Scheduler For Configurable Logic System Performing Simultaneous Communications and ~~Communication~~Computation" to Selvidge et al., disclose methods for efficiently routing among PLDs signals under timing constraints. U.S. Patent ~~5,820,348~~5,802,348, entitled "Logic Analysis System For Logic Emulation Systems" to Stewart et al., provides logic analyzer functions to be used in analyzing the operations within the emulation circuit.

Amend the paragraph spanning from p. 2, ln. 18, to p. 3, ln. 6, as follows:

In a large logic circuit, circuit operations are controlled by one or more clock signals. Thus, proper handling of clock signals is important to achieve ~~a~~ successful emulation of a logic circuit. For example, U.S. Patent 5,649,176, entitled "Transition Analysis And Circuit Resynthesis Method and Device For Digital Circuit Modeling," discloses using an internal clock signal outside of the timing signals of the logic circuit to control the internal operations of the emulation circuit. In a typical emulation system, a single clock signal is

distributed throughout the emulated logic circuit to provide synchronization. While this clock distribution scheme is conventional in an emulation circuit configured in PLDs in very close proximity (e.g., PLDs on a single circuit board, or on different circuit boards interconnected on a single backplane bus), such a clock signal cannot be provided between PLDs separated by a relatively large distance (e.g., PLDs on circuit boards on different ~~chassises~~chassis) or at high clock frequencies, such as those used for multiplexed data transport. In such a system, there may be large clock skews at different points of the system relative to the clock period that cannot be reliably estimated. Thus, practically, those different points of the system are effectively asynchronous relative to each other. Thus, there is a need for a reliable method for transporting data between distinct ~~synchronous~~ asynchronous components of a system, without relying on a common clock signal distributed throughout.